LABORATORY MANUAL

FOR

Lab Course EL 491

Electronics Circuit Design Laboratory

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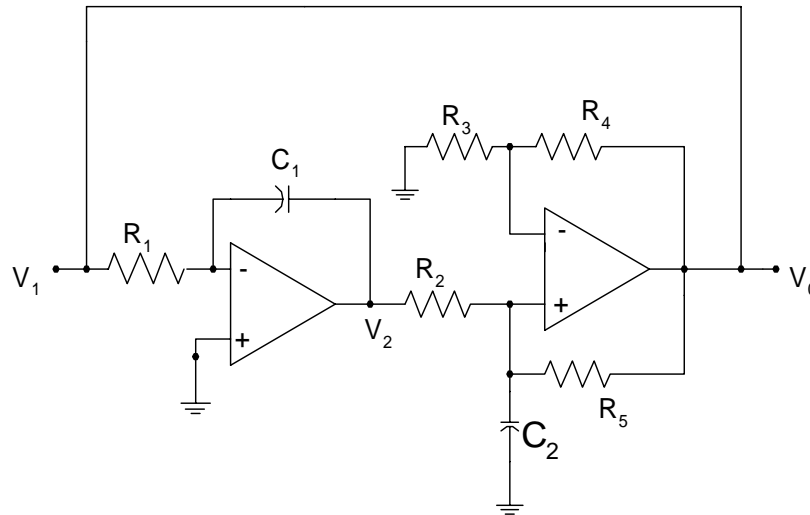**NB**:- This laboratory manual is also available on the Internet and can be downloaded from:-

http://hadialikhan.tripod.com/lab491.pdf

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Electronic Circuits Design Laboratory

Lab. Course EL – 491

Experiment No. 01 (Quadrature Oscillator)

Object:- ***Design and Experimentally Verify an Opamp-based Quadrature Oscillator for a frequency of ………….. Hz***

Circuit Diagram:-

Theory:-   On analyzing the circuit of the quadrature oscillator, shown above, the **condition**

of the oscillation may be written as : $\dfrac{R_4}{R_3} = \dfrac{R_5}{R_2}$ -------   ------------   (1)

And the frequency of oscillation can be expressed as $\omega^2 = \dfrac{1 + \dfrac{R_4}{R_3}}{R_1 R_2 C_1 C_2}$,

or, $f = \dfrac{1}{2\pi} \sqrt{\dfrac{1 + \dfrac{R_4}{R_3}}{R_1 R_2 C_1 C_2}}$,

Taking $R_3 = R_4$ and $C_1 = C_2 = C$, $f = \dfrac{1}{2\pi C} \sqrt{\dfrac{2}{R_1 R_2}}$ -----   -----   (2)

Design:-

For design frequency (given), assume appropriate values of R1 & C,

and calculate R_2 = …………….. KΩ,

Corresponding to the nearest available value of the resistor, calculate f by back calculations.

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Observations:-

Use a pot of 10 KΩ for (R_3 + R_4) and adjust it to get the output waveform Vo. Once the output Vo is obtained corresponding to the particular values of R_1 and R_2, replace R_1 by a few discrete values of resistors such as 2.2 KΩ, 3.3 KΩ, 4.7 KΩ etc., and measure the frequency of V_o corresponding to each of these values and verify that the frequency is changing but the phase difference between V_o and V_2 is always 90^0.

R_1 (KΩ)	Time period (μs)	Practical value of frequency (KHz)	Theoretical value of frequency (KHz)

Sample Calculations:

Designed frequency = -------- KHz
Measured frequency = -------- KHz

%age error = ----- %

Plot a curve between R_1 & f .

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Electronic Circuits Design Laboratory

Lab. Course EL – 491

Experiment No. 02 (Switch Capacitor)

Object:- *Design and Experimentally Verify a first-order low pass switched capacitor section for a cut-off frequency of ………….. Hz*

Theory:-

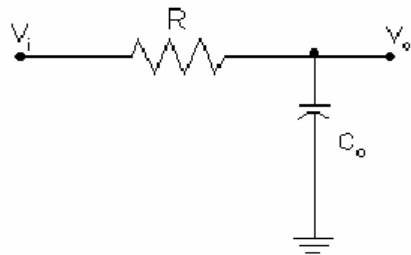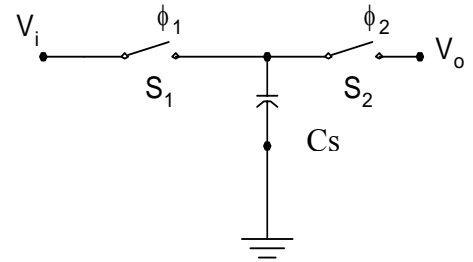Fig.1   Fig. 2

The resistor R, in figure 1 can be simulated by a capacitor C_s, connected between two switches S_1 and S_2, turning ON and OFF by the two non-overlapping pulses ϕ_1 and ϕ_2 at the switching frequency f_C, as shown in figure 2.

The transfer function of the above low-pass section is given by the expression:

$$\frac{Vo}{Vi} = \frac{(1/RC_o)}{s+(1/RC_o)} \text{ , which gives } \omega_o = \frac{1}{RC_o} \text{ ,}$$

Therefore, $f_o = \dfrac{1}{2\pi RC_o}$ .... (1)

With reference to figure 1 & 2, the current through R is $i = C_s \dfrac{dv}{dt} = C_s \dfrac{V_1 - V_2}{T_C} = \dfrac{V_1 - V_2}{R}$.

Therefore, $R = \dfrac{T_C}{C_s} = \dfrac{1}{C_s f_C}$, ... (2),

Substituting the value of R obtained from equation (1) into equation (2) yields

$f_o = \dfrac{C_s f_C}{2\pi C_o}$.

or,

$$\boxed{\frac{f_C}{f_o} = 2\pi \left(\frac{C_o}{C_s}\right)}$$

Take $\dfrac{f_C}{f_o} = $ (2 to 30) ,

**Design**: For your design frequency $f_o = $ ------ Hz , (given), Choose $C_o = $ --------- µF,

Now using $f_c = 30 f_o$, Calculate $C_S = $ … , Take $C_S = $ -------- µF, & calculate $f_C = $ ----

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The practically used values are

C_o = ------ μF
C_S = ------ μF
f_o = ------ KHz
f_C = ----- KHz

Note:- Use a NAND gate (TTL IC 7400) as an inverter (NOT gate), to get non-overlapping pulses and a CMOS IC, CD 4066 for the two switches. (Ref:- Pin configurations of the two ICs), where ϕ_1 is the clock pulse of freq. $= f_c$

ϕ_1 ⟶ ◁○ ϕ_2

Inverter
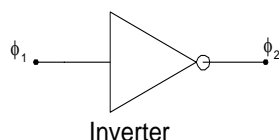
Observations:- V_i = -------- mV, and f_c = -------- KHz,

S. No.	Signal freq. f_i (Hz)	V_o = O/P Voltage (mV)	Gain = (V_o/ V_i)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			

Plot the frequency response curve (gain versus frequency),

Result:-

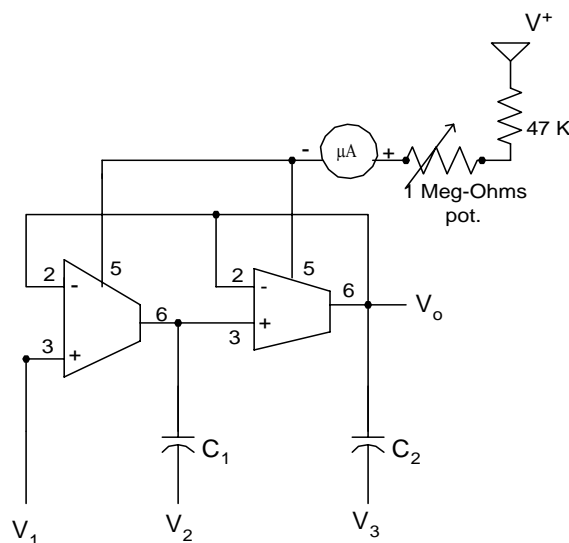Practical value of the cut-off frequency obtained from the graph plotted is 490 Hz.

Designed value (given) = ------ Hz.

Hence, the percentage error   = -------- %.

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Experiment No. 03 (OTA Multi-function Filters)

Object   **Analyze, design and experimentally verify the OTA – c multi-function filters for the LP, HP, BP and BE responses for a cut-off (pole) frequency of …… KHz & Q = 1.**

Circuit Diagram:-

Theory and Assumptions:-

$$V_0 = \frac{s^2 V_3 + s \frac{g_{m2}}{C_2} V_2 + \frac{g_{m1}}{C_1} \frac{g_{m2}}{C_2} V_1}{s^2 + s \frac{g_{m2}}{C_2} + \frac{g_{m1}}{C_1} \frac{g_{m2}}{C_2}} \qquad (3.1)$$

$$BW = \frac{\omega_0}{Q} = \frac{g_{m2}}{C_2} \quad ; \quad \omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \qquad (3.2)$$

$$Q = \sqrt{\frac{g_{m1} C_2}{g_{m2} C_1}} \quad ; \quad g_{m1} = g_{m2} = \frac{I_B}{2V_T} = 19.23 I_B \qquad (3.3)$$

Assumptions:- $g_{m1} = g_{m2} = g_m = \frac{I_B}{2V_T} = 19.23 I_B,$ $C_1 = C_2 = C,$ $Q = 1$

The cut-off (pole) frequency is given by:-

$$f_0 = \frac{19.23 I_B}{2\pi C} = 3.062 \frac{I_B}{C} \qquad \text{---------} \qquad \text{-------------} \quad (1)$$

The Band-width (BW) = $\frac{\omega_o}{Q} = 2\pi f_o,$

$H_{HP} = H_{LP} = H_{BP} = H_{BE} = 1,$

Operating Conditions:-

For LPF:- $V_i = V_1$, & $V_2 = V_3 = 0$

For HPF:- $V_i = V_3$, & $V_2 = V_1 = 0$

For BPF:- $V_i = V_2$, & $V_1 = V_3 = 0$

For BEF:- $V_i = V_1 = V_3$, & $V_2 = 0$

Adjustment of I_B by R_x

$R_T = (R_x + R)$, where R_x = variable resistor and R = fixed resistor

R_T (KΩ)	100	150	200	300	600
Total I_B (µA)	150	100	75	50	25

DC Biasing Supply range = Symmetrical dual (+/- 6 to 18) volts

DC Biasing Supply used = Symmetrical dual (+/- 15) volts

Design:-

Given f_0 = ------- KHz,   Assume I_B = ----- µA

Calculate C = ------- µF,   BW = ($874.1 \times 10^6 \, I_B$) Hz ,

Test the circuit band-width for I_B = 25 µA, 50 µA and 100 µA.

Observations :-

V_0 = ----- mV and I_B = ----- µA,

1. Readings for LPF:- V_i = 20 mV

S. No.	f_i (KHz)	V_o (mV)	Gain (A) = V_o / V_i
1.	0.1		
2.	0.2		
3.	0.5		
4.	1.0		
5.	1.5		
6.	1.9		
7.	2.5		
8.	3.2		
9.	4.2		
10.	5.0		
11.	5.5		
12.	7.0		

2. Readings for HPF:- V_i = 20 mV

| S. No.	f_i (KHz)	V_o (mV)	Gain (A) = V_o / V_i
1.	0.1		
2.	0.2		
3.	0.5		
4.	1.0		
5.	1.5		
6.	1.9		
7.	2.5		
8.	3.2		
9.	4.2		
10.	5.0		
11.			

Similarly take observations for BPF and Band Elimination (Notch) filters.

Plot the frequency response curves for LPF, HPF, BPF & BEF.

Report:- 1. Derive the expressions for the operating conditions.
   2. Comment on the frequency responses obtained.

Testing an OTA (CA3080)

Connect the OTA under test as shown in the following circuit diagram:-
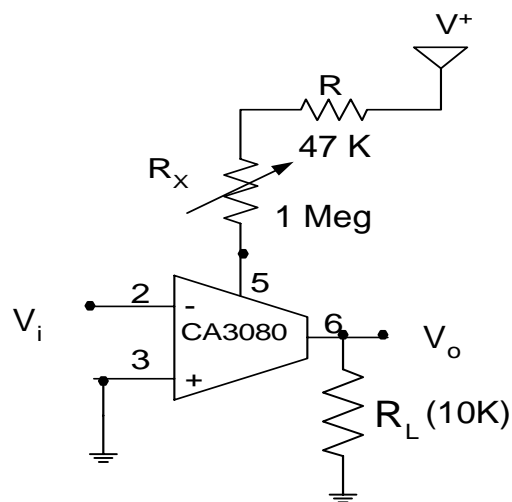
1. Apply a sinusoidal signal of amplitude 50 mV_{p-p} and frequency 2.0 KHz at Vi.
2. Observe the output signal.
3. If it is of opposite phase of the input and its amplitude is increasing by adjusting the variable resistance, then the OTA under test is all right.
4. If no signal is observed at the output, or the amplitude does not change by variable resistance, then the OTA is defective.

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Experiment No. 04 (Precision Rectifier)

Object:-   **Design and experimentally verify the Full-wave and the Half-wave precision rectifier using bi-phase amplifier. Plot the output DC voltage versus input RMS voltage for the input signal between 0 volt and 1 volt.**

Circuit Diagram:-
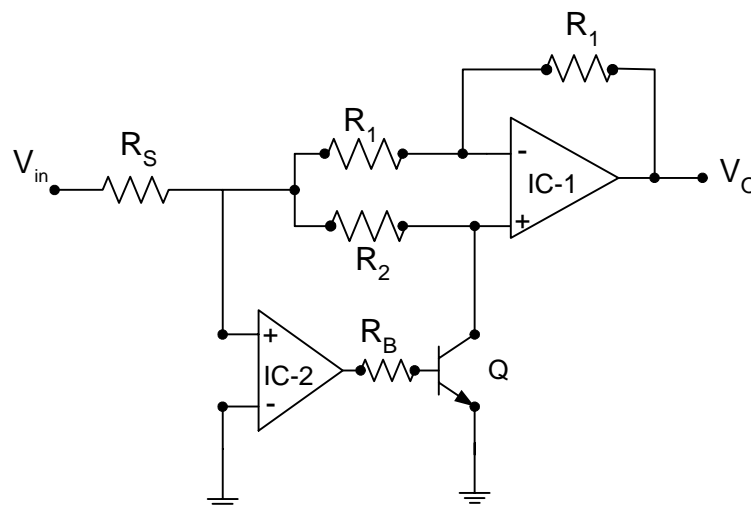
$V_o = - V_{in}$, when Q is ON,

$V_o = + V_{in}$, when Q is OFF

Typically, $V_{in} = 0.2$ Volt$_{p-p}$ / 1.0 KHz Sine wave.

For Half-wave rectification, replace R1 by a short-circuit between pins # 2 and 6 of the IC-1.

1. Find the minimum input signal level for proper rectification at f = 200 Hz.

2. Find the maximum signal frequency for proper rectification at $V_{in} = 1.0$ Volt$_{p-p}$

3. Trace the output waveforms for half-wave and full wave rectifiers.

Components Used:-
1) Opamp 741 (IC-1 & (IC-2)
2) NPN Transistor (Q) BC 147
3) Resistors:

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Experiment No. 5 (CFA)

Object:-   Design an all pass section using CFA (AD844) for a pole frequency ω_p (= ω_z) = 2 πf_o (f_o = gp-no KHz). Plot the frequency response of the designed AP section (*magnitude and phase of V_{o2} with respect to V_i, versus frequency*).

Circuit Diagram:-
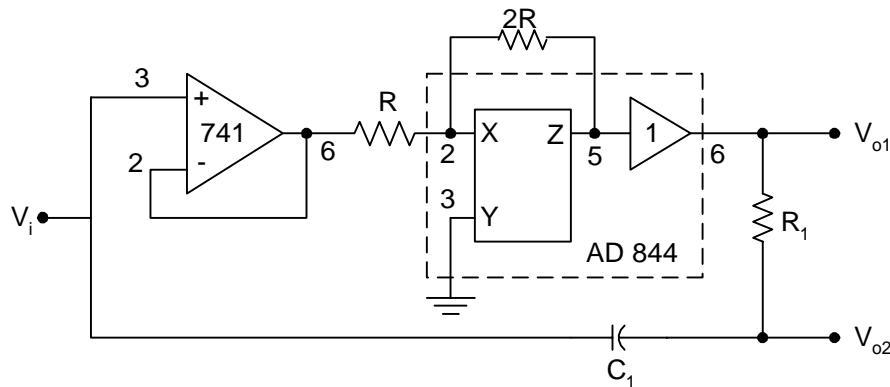
Design Equations:-

$$\frac{V_{o1}}{V_i} = -1 \ , \qquad\qquad\qquad ---- \ ---- \ (1)$$

$$\frac{V_{o2}}{V_i} = \frac{s - \dfrac{1}{R_1 C_1}}{s + \dfrac{1}{R_1 C_1}} \qquad\qquad ---- \ ---- \ (2)$$

The pole frequency $\boldsymbol{\omega_p} = \boldsymbol{\omega_z} = \dfrac{1}{R_1 C_1} \qquad ---- \ ---- \ (3)$

(R = 10 KΩ, R_1 = 22 KΩ)

(V_i = **0.4 $V_{p\text{-}p}$ / 1.5 KHz** Sine wave may be used for initial testing of the designed circuit).

Ratings of AD844 (60 MHz, 2000 V/µs Monolithic Op Amp):-

Wide-range of Biasing Power Supplies: ± 4.5 V to ± 18 V; Capable of high o/p drive of ± 50 mA to50 Ω; Low offset voltage: 150 µV; Low Quiescent current: 6.5 mA; Large BW : 60 MHz at Gain of -1;

Pin Connections:-

8-Lead PDIP (N) and CERDIP (Q) Packages

NULL | 1   • AD844   8 | NULL
- IN (X) | 2   —   7 | +V_S
+ IN (Y) | 3   +   6 | OUTPUT
–V_S | 4   TOP VIEW (Not to Scale)   5 | TZ
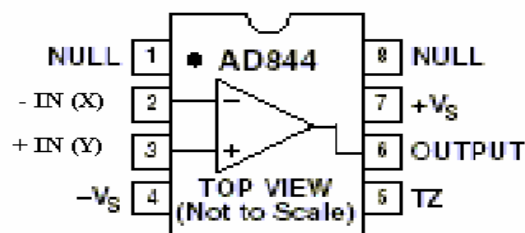
Experiment No 06 (Opamp based Multi-function filter)

Object:- Analyze, design and experimentally verify   the OPAMP based multifunction filter to realize low pass, high pass, band pass and band elimination responses for given cutoff (pole) frequency f_o = ….. KHz.

Circuit Diagram:-

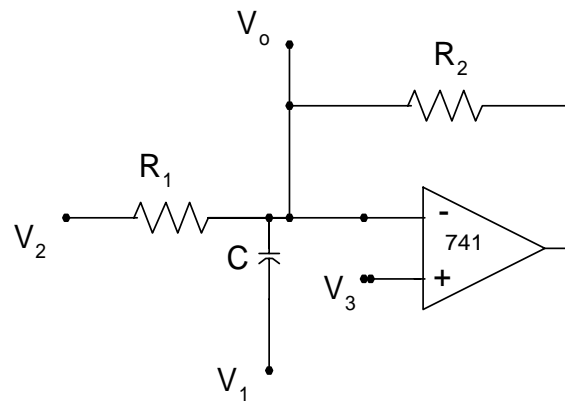
Theory and Analysis:-

On analyzing the circuit, the expression for V_o can be written as:

$$V_o = \frac{s^2 V + s\dfrac{V_2}{R_1 C} + V_3 \dfrac{B}{R_2 C}}{s^2 + \dfrac{s}{C}\left[\dfrac{1}{R_1} + \dfrac{1}{R_2}\right] + \dfrac{B}{R_2 C}} \quad , \quad \text{-----} \quad \text{-----} \quad \text{-----} \quad (1)$$

where B = unity-gain band width of the opamp.

$$\omega_0 = \sqrt{\frac{B}{R_2 C}} \quad , \qquad Q = \frac{R_1}{R_1 + R_2}\sqrt{BCR_2}$$

Design:- Expression for $f_o = \dfrac{1}{2\pi}\sqrt{\dfrac{B}{R_2 C}}$,   -----   -----   (2)

Note:- For Opamp 741, select B in the range (0.4 – 1.5) MHz.

Operating Conditions:

With reference to the eqn (1) above, the circuit will be working as a multi function filter under the following conditions:

For Low pass filter:- $\qquad$ $V_1 = V_2 = 0$, and $V_3 = V_{in}$,

For High pass filter:- $\qquad$ $V_3 = V_2 = 0$, and $V_1 = V_{in}$,

For Band pass filter:- $\qquad$ $V_1 = V_3 = 0$, and $V_2 = V_{in}$,

For Band Elimination filter:- $\qquad$ $V_2 = 0$, $\qquad$ and $V_1 = V_3 = V_{in}$,

where 0 stands for grounded and V_{in} for the input signal.

Observations:
Given $f_0 =$ …….. KHz
Take $R_1 = R_2 =$ ---- KΩ
Calculate C = ----- nF, Use the nearest available value of C = -------- μF,
By back calculation, $f_0 =$
$V_{in} =$ -------- volts $_{p-p}$

(i) Readings for low pass filter:-

S. No.	Freq. of V_{in} (Hz)	Amplitude of $V_{o\ p-p}$ (mV)	Gain, $A = \dfrac{V_o}{V_{in}}$

Similarly tabulate:-

(ii) Readings for high pass filter:-

(iii) Readings for band pass filter:-

(iv) Readings for band elimination filter:-

Measure f_0 from the frequency-response curve.

Report:- Plot frequency response of each filter on the same semi-log graph paper and verify the designed cutoff frequency f_o. Also give your comments on the results and carry out circuit analysis.

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APPENDIX - I

Some Common Precautions

Care should be taken to observe the following Precautions while performing experiments ON the circuits employing Electronic Devices:-

1. Before connecting the device into the circuit, always ensure that the device is perfectly working; that is, it should have already been tested separately in its test-circuit.

2. Always connect the device/IC carefully and correctly into the circuit being assembled on the Breadboard to avoid any loose or incorrect connection leading to the damage of the device.

3. While connecting the device into the circuit on the breadboard, ensure that no DC supply or signal is connected to that circuit. (Keep power supplies and signal generators OFF).

4. When the device has been correctly connected into the circuit, only then turn ON the DC supply and the signal generators in this order:- "Firstly turn ON the Power Supply; then turn ON the signal generator".

5. Don't forget to check the output voltage of the DC power supply before connecting it to the circuit, and adjust it to proper value conforming to the device specifications.

6. Don't forget to adjust the amplitude of the signal to be connected to the device, to its proper value, always below the maximum signal level specified in the device data sheet, to avoid the consequent damage to the device already checked and found OK.

7. Take extra care while using the costly and sensitive devices like OTAs and Current conveyers, that is, read thoroughly their specifications given in their datasheets, and never violate any rating of the device.

8. Before replacing any device or component on the bread-board, turn-OFF the signal generator first and then turn-OFF the power supplies connected to the circuit, and then replace the device or component; and after replacement, switch ON the power supply first & then switch ON the signal generator.

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APPENDIX – II

**Pin Connections and the Specifications of the ICs : CD 4066 and OTA CA 3080**

CD4066BM/CD4066BC Quad Bilateral Switch

Features

- Wide supply voltage range   3V to 15V
- High noise immunity   0.45 V_{DD} (typ.)
- Wide range of digital and   ±7.5 V_{PEAK}
  analog switching
- "ON" resistance for 15V operation   80Ω
- Matched "ON" resistance $\Delta R_{ON} = 5Ω$ (typ.)
  over 15V signal input
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF"   65 dB (typ.)
  output voltage ratio   @ $f_{is} = 10$ kHz, $R_L = 10$ kΩ
- High degree linearity   0.1% distortion (typ.)
  High degree linearity   @ $f_{is} = 1$ kHz, $V_{is} = 5V_{p-p}$,
  High degree linearity $V_{DD} - V_{SS} = 10V$, $R_L = 10$ kΩ

Dual-In-Line Package

Top View
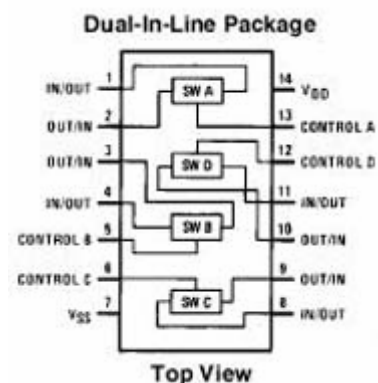
Schematic Diagram:-
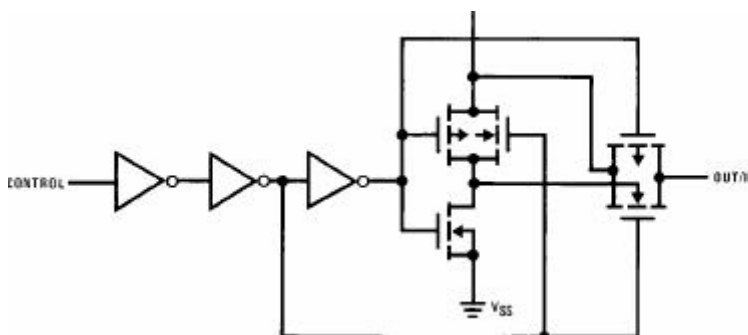
Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD}+0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

For further details, refer to the manufacturer's Datasheet
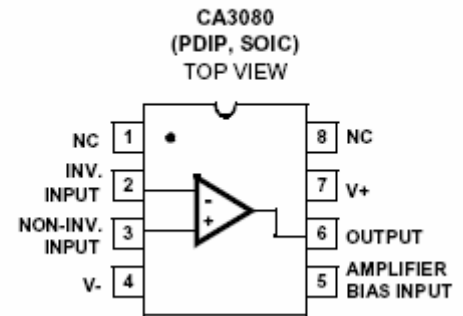
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CA 3080
2MHz, Operational Transconductance Amplifier (OTA)

Features

- Slew Rate (Unity Gain, Compensated) 50V/μs
- Adjustable Power Consumption . . . . .10μW to 30μW
- Flexible Supply Voltage Range . . . . ±2V to ±15V
- Fully Adjustable Gain. . . . . .0 to $g_M R_L$ Limit
- Tight g_M Spread:
  - CA3080. . . . . 2:1
  - CA3080A 1.6:1
- Extended g_M Linearity . . . . 3 Decades

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminal). 36V
Differential Input Voltage 5V
Input Voltage . . . . V+ to V-
Input Signal Current. 1mA
Amplifier Bias Current (I_{ABC}). 2mA
Output Short Circuit Duration (Note 1). . . . . No Limitation

Pinouts

CA3080
(PDIP, SOIC)
TOP VIEW

Take I_B < 500μA & V_i < 100 mV

The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class-A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (gM) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50V/μs), which makes them especially useful for multiplexer and fast unity-gain voltage followers. These types are especially applicable for multiplexer applications because power is consumed only when the devices are in the "ON" channel state.

For further details, refer to the manufacturer's Datasheet

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